

# CLAIMS

We claim:

1           1.    A sense amplifier circuit comprising:  
 2           a sense amplifier coupled to a first input line and a  
 3   second input line and adapted to receive an enable signal,  
 4   wherein the enable signal controls whether the sense amplifier  
 5   is enabled;  
 6           a first inverter coupled to the first input line and  
 7   adapted to provide a first output signal;  
 8           a second inverter coupled to the second input line and  
 9   adapted to provide a second output signal; and  
 10          a logic gate adapted to receive the first output signal and  
 11   the second output signal and to provide a trip signal.

1           2.    The sense amplifier circuit of Claim 1, wherein the  
 2   trip signal indicates when the sense amplifier has read a data  
 3   value provided on the first input line and/or the second input  
 4   line and when the first input line and the second input line are  
 5   precharged.

1           3.    The sense amplifier circuit of Claim 1, further  
 2   comprising a latch adapted to store a result provided by the  
 3   first output signal or the second output signal, wherein the  
 4   result is stored by the latch when the trip signal transitions  
 5   to a first value.

1           4.     The sense amplifier circuit of Claim 1, further  
2 comprising:

3           a latch adapted to store a result provided by the first  
4 output signal or the second output signal, wherein the result is  
5 stored by the latch when the trip signal transitions to a first  
6 value; and

7           a precharge circuit adapted to precharge the first input  
8 line and/or the second input line, wherein when the enable  
9 signal enables the sense amplifier, the precharge circuit stops  
10 precharging the first input line and/or the second input line.

1           5.     The sense amplifier circuit of Claim 1, further  
2 comprising:

3           a latch adapted to store a result provided by the first  
4 output signal or the second output signal, wherein the result is  
5 stored by the latch when the trip signal transitions to a first  
6 value;

7           a precharge circuit adapted to precharge the first input  
8 line and/or the second input line when the enable signal  
9 transitions to a first value, with the trip signal transitioning  
10 to a second value when the first input line and/or the second  
11 input line reach precharge values; and

12          a column multiplexer adapted to select which data lines to  
13 couple to the first input line and/or the second input line,  
14 wherein when the enable signal enables the sense amplifier by  
15 transitioning to a second value, the precharge circuit stops  
16 precharging the first input line and/or the second input line  
17 and the column multiplexer couples at least one data line to the  
18 first input line and/or the second input line.

1           6.     The sense amplifier circuit of Claim 5, further  
2     comprising a global precharge circuit adapted to precharge the  
3     data lines.

1           7.     The sense amplifier circuit of Claim 1, further  
2     comprising a sense amplifier circuit controller adapted to  
3     control one or more of the sense amplifier circuits by  
4     controlling the enable signal and monitoring the trip signal of  
5     each of the sense amplifier circuits.

1           8.     The sense amplifier circuit of Claim 1, wherein the  
2     first and second input lines are couplable to bitlines of a  
3     memory array, wherein the memory array comprises a number of  
4     sense amplifier circuits adapted to read data stored in the  
5     memory array.

1           9.     A memory array comprising:

2           a plurality of sense amplifiers adapted to read data  
3     provided on bitlines;

4           a plurality of corresponding precharge circuits adapted to  
5     precharge the bitlines coupled to the sense amplifiers;

6           a plurality of corresponding inverters coupled to the  
7     bitlines and adapted to provide output signals based on signal  
8     levels on the bitlines coupled to the sense amplifiers;

9           a plurality of corresponding logic gates adapted to receive  
10    the output signals from the corresponding inverters and to  
11    provide trip signals based on the output signals; and

12 a plurality of corresponding latches adapted to store the  
13 output signals from one of the corresponding inverters under  
14 control of the corresponding trip signals, wherein the trip  
15 signals transition to a first value when the corresponding  
16 bitlines are precharged and transition to a second value when  
17 the corresponding sense amplifiers read the data on the  
18 corresponding bitlines.

1 10. The memory array of Claim 9, wherein the sense  
2 amplifiers are disabled when the corresponding trip signals  
3 transition to the second value.

1 11. The memory array of Claim 9, wherein the precharge  
2 circuits are enabled to precharge the corresponding bitlines  
3 when the corresponding trip signals transition to the second  
4 value.

1 12. The memory array of Claim 9, further comprising a  
2 plurality of sense amplifier controllers with each associated  
3 with one or more of the sense amplifiers, wherein the sense  
4 amplifier controllers control the enabling and disabling of the  
5 associated sense amplifiers and the associated precharge  
6 circuits based on the associated trip signals.

1 13. The memory array of Claim 12, further comprising a  
2 plurality of column multiplexers adapted to couple selected data  
3 lines to the bitlines of the corresponding sense amplifiers,  
4 wherein the column multiplexers are enabled by the associated  
5 sense amplifier controllers.

1        14. A method of reading data from data lines, the method  
2 comprising:

3        disabling a sense amplifier coupled to the data lines;

4        precharging the data lines;

5        providing a first signal value via inverters coupled to the  
6 data lines when the data lines are precharged;

7        providing the data on the data lines after the first signal  
8 value is provided;

9        enabling the sense amplifier to read the data placed on the  
10 data lines after the first signal value is provided; and

11       providing a second signal value via the inverters coupled  
12 to the data lines when the sense amplifier has read the data  
13 placed on the data lines.

1       15. The method of Claim 14, further comprising repeating  
2 the method by disabling the sense amplifier and precharging the  
3 data lines after the second signal value is provided.

1       16. The method of Claim 14, further comprising storing an  
2 output signal provided by one of the inverters when the second  
3 signal value is provided.

1       17. The method of Claim 14, further comprising disabling  
2 the precharging after the first signal value is provided.